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RADAR STUDIES OF ARCTIC ICE AND DEVELOPMENT OF A REAL-TIME ARCT--ETC(U)
JAN 76 J A SCHELL, B R JEAN, W C HULSE N60921-74-C-0008
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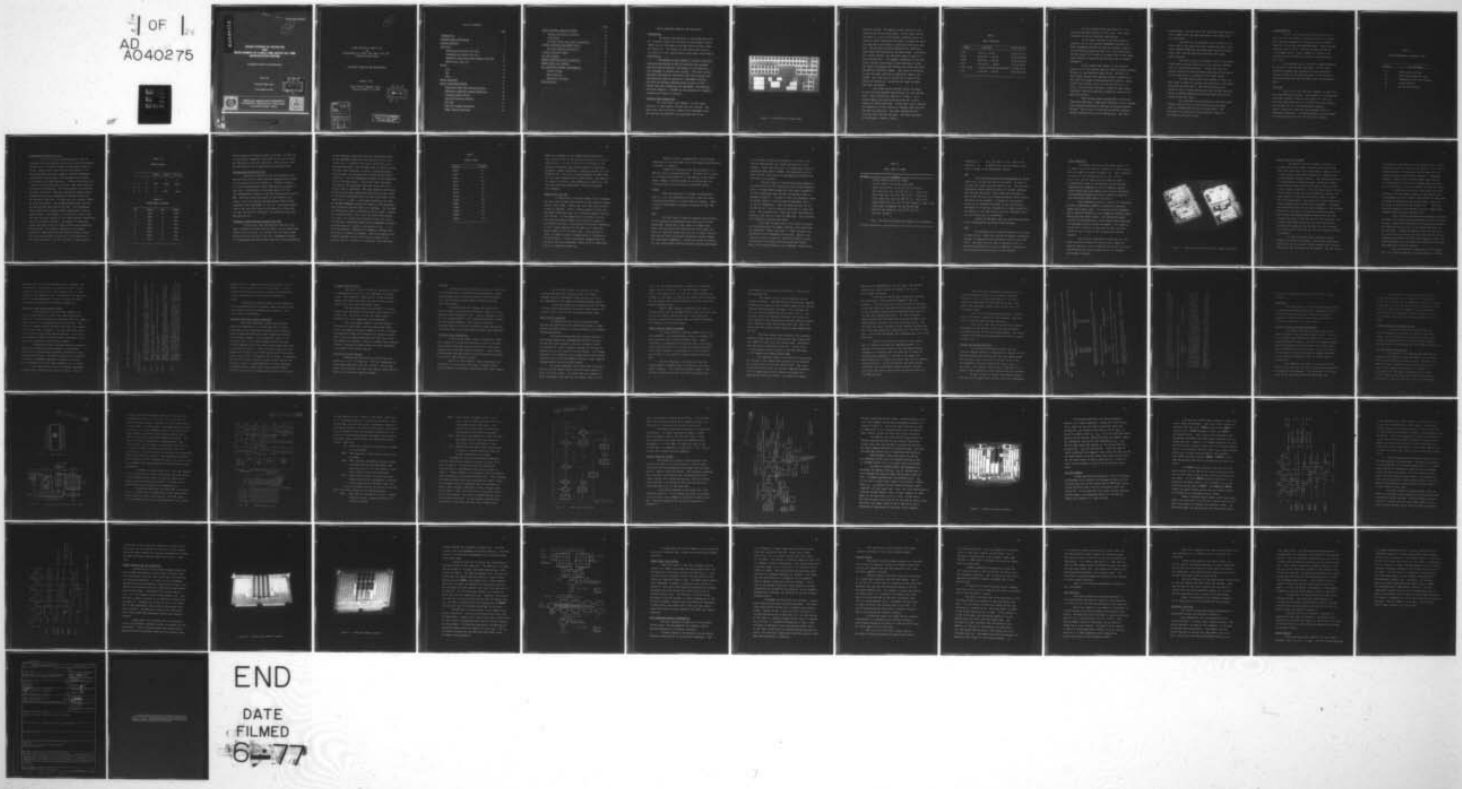

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RADAR STUDIES OF ARCTIC ICE AND DEVELOPMENT OF A REAL-TIME ARCTIC ICE TYPE IDENTIFICATION SYSTEM

PROCESSOR OPERATION AND MAINTENANCE

January 1976

Naval Surface Weapons Center

Contract N60921-74-C-0008

TEXAS A&M UNIVERSITY
REMOTE SENSING CENTER
COLLEGE STATION, TEXAS

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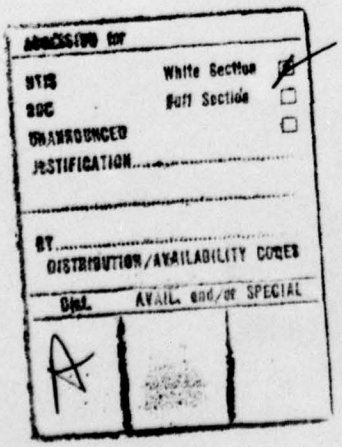

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RTICS PROCESSOR OPERATION AND MAINTENANCE

INTRODUCTION

The Remote Sensing Center at Texas A&M University has conducted studies for the Naval Surface Weapons Center (NSWC) and has developed a real-time special purpose radar data processor. The purpose of this processing system is to provide ice type identification using radar scatterometer measurements.

The purpose of this manual is to give a detailed technical description of how the processor was designed and built and to provide a description of its operation. This document is divided into sections. The first section describes the operator interaction with the processor and the processor modes of operation. Subsequent sections describe the hardware implementation in terms of the analog sign-sense subsystem, CPU and memory subsystem and the Power Supplies. Included in the appendix are schematic diagrams and software flowcharts.

OPERATOR PANEL DESCRIPTION

The front panel (see Figure 1) of the signal processor is functionally divided into two sections. The upper four rows of switches comprise the programmer interface and are not required for operational use of the

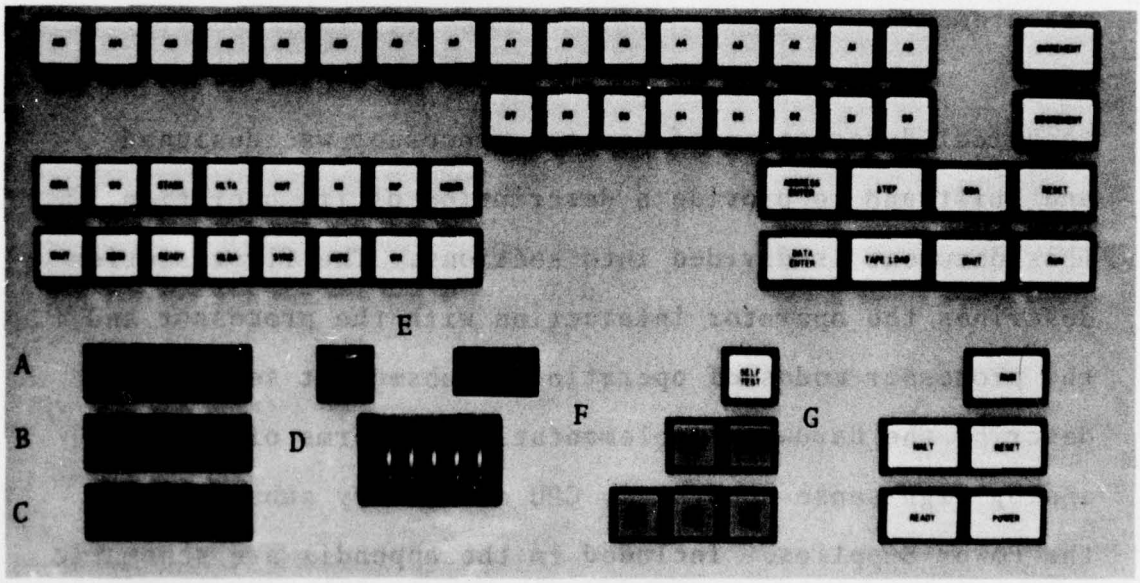


Figure 1. RTICS Processor Front Panel

processor system. The operator panel consists of the lower portion of the front panel. To the lower left of the panel is a set of six switches (labeled A and B in Figure 1) which control the selection of angles for which the processor will provide a scattering coefficient output. The top three switches labeled 0/20, 20/40 and 40/60 allow specification of the angle range. Activation of a switch includes the indicated range of angles in the processed data. For example, activation of the 0/20 switch includes processing of data from angles within the range 0-20 degrees and similarly for 20/40 and 40/60 include the additional ranges. This setup is inclusive in that for each selection an additional range is included. Note that for all selections a total of ten angles are processed. Increasing the range decreases the angle resolution.

The second row of switches within the group of nine sets the operator specification for fore and aft data. These switches are labeled X, Y and Z. The X switch enables fore data processing and the Y switch enables aft data processing. If both the X and Y switches are enabled or if the Z switch is enabled, then fore and aft data are processed. Any other combination also processes both fore and aft data. The angle selection for each mode is shown in Table I.

TABLE I

ANGLE SELECTION

Range	Fore/Aft	Fore and Aft
0-20	2,4,6,...,18,20	5,10,15,20,25
20-40	20,22,24,...,36,38	20,25,30,35,40
40-60	40,42,44,...,56,58	40,45,50,55,60
0-40	4,8,10,12,...,36,40	5,15,25,35,45
0-20, 40-60	5,10,15,20,25,40,45,50,55,60	5,10,20,45,55
0-60	10,15,20,...,50,55	10,25,35,45,55

The two switches below the group of six (C) have no processing function at this time. They remain available for future processor modification.

In the center portion of the front panel is located a set of five decimal thumbwheel switches (D). These thumbwheel switches provide for operator input to the processing program and their use is described later. The MDR switch (E) located to the upper left of the thumbwheel switches is used during operator entry of program parameters.

In the bottom right center of the processor panel are five red warning lamps (F) which indicate possible failures in the processor/radar system. The ROLL and DRIFT lamps indicate that decoded aircraft parameters of roll and drift angles exceed prespecified limits. These limits are currently set at 3.5° of roll and 8.5° of drift. The processor continues to function under these conditions which are generally accepted as excessive for good data results.

Other warning lights include RDR, a radar fail lamp which indicates a significant unbalance in the incoming radar signal, and ANA which indicates an analog processor failure. This failure is detected by reduced isolation between simulated fore and aft analog data. The final

warning lamp is the processor fail lamp (DPR) which indicates that a memory error has been detected by the system self-test algorithms.

The final set of switches (G) are located on the lower right of the panel and these include the Power on-off switch labeled POWER and four additional function switches, RESET, IDLE, RUN and HALT, which determine the actual processing mode.

The RESET switch is a hardware reset of the entire system which initiates execution of the processor software from its initialization point. A reset will cause immediate cessation of the processing function and initialization of the process or software to the "IDLE" state.

The IDLE switch causes the software to enter the IDLE state in which the operator specification of the flight processing can take place. The RUN switch places the processor into a signal analysis mode and the HALT function causes an orderly shutdown of the processing function and return to the IDLE state.

This concludes the description of the front panel. Operator specification of and control over processing modes is accomplished only by the front panel. The procedures for operation of the processor system are described in the next section.

SYSTEM OPERATION

In this section the detailed operational procedures for the scatterometer signal processor are provided. These include procedures for self-test and for operator functions in the IDLE, RUN and HALT modes. Power provided should be 115v at 60 Hz. Turn on the processor by way of the POWER switch. Depress RESET to initialize the software and to activate the system central processing unit (CPU).

The processor may be tested for proper operation by placing it into the self-test mode. In this mode, software procedures are initiated to allow interactive testing of most of the major functions of the processor. To activate self-test turn the SELF switch on and depress RESET.

SELF-TEST

Each test in the self-test sequence is identified by an individualized display. The sequence is distinguished from other software states by the prefix "F", thus the processor identifies that it is in the first test sequence by a display of "F1" on the hexidecimal display. Table II identifies each self-test procedure with its appropriate numbering. A system functional test procedure is described which utilizes the self-test software.

TABLE II

SYSTEM PERFORMANCE ASSURANCE TESTS

Display	Test Performed
F1	Panel Switch on State
F2	Panel Switch Bank Off State
F3	Thumbwheel Switch Test-Display
F4	System RAM Test
F5	System ROM Checksum

Configuration Switch Test (F1)

In this test, all warning indicators will be turned On and, upon operator direction, system configuration switches will be read and checked to determine an On condition. Observe entry into the test by display of "F1" which identifies this test segment. Observe illuminated condition on warning lamps. Set configuration switches On and depress the MDR indicator. If the system identifies a switch in the Off position, an error code identifying the switch will be displayed. The error display is identified in Tables III and IV. The most significant display digit identifies the row of configuration switches which does not conform to the test. In this case, all switches should be in an on position. The second display digit describes how the switches were read by the CPU. This hexidecimal digit identifies the binary number representation of the switch states. For example, if in this test switch X was off, then an error display of "23" would register identifying row "2" as having a failure. The number "3" identifies switch positions 0 and 1 as being on and switch position 3 as being off. All switches should be on; therefore, switch X is identified from the table as being at fault. An error will register in this test if the switch is in the wrong position, or if the circuitry to that switch is

TABLE III

ERROR DISPLAY

		Binary	Digit	Position
		3	2	1	0
I	1	0	0/20	20/40	40/60
D	2	0	X	Y	Z
#	4	0	0	Fore	Land

TABLE IV

HEXIDECIMAL TO BINARY

Hex	Binary	Hex	Binary
0	0000	8	1000
1	0001	9	1001
2	0010	A	1010
3	0011	B	1011
4	0100	C	1100
5	0101	D	1101
6	0110	E	1110
7	0111	F	1111

faulty causing an incorrect sense to be read. If the test is successfully completed, there will be no error display and the next test will be initiated. The processor turns the MDR function off in preparation for the next test.

Configuration Switch Test (F2)

During this portion of the test procedure, all warning flags will be turned Off and configuration switches will be tested for an Off condition. Observe a display of F2 on the hexidecimal display indicating initiation of this test. Also observe all warning lamps to be Off. Set configuration switches to the Off condition and activate MDR. Incorrect switch positions or read failures will result in an error display identifying the faulty switch function in the same manner as test F1. Successful completion of the test will result in no display of errors and the next test will be initiated. The processor turns the MDR function off.

Thumbwheel and Hexidecimal Display Test (F3)

In this test, the read function from the front panel thumbwheel switches and the display to the hexidecimal readout will be tested. To initiate the test depress MDR. During the first portion of the test, thumbwheel switches are interrogated and the results from this read are displayed.

In this portion of the test, the most significant digit on the thumbwheel identifies the switch position being tested (e.g., 1 indicates the least significant digit is read and displayed). The switches will be tested in order to assure their operation in the 0, 7 and 8 positions, which accounts for all data bits in both the On and Off conditions. Set the thumbwheel switches to read 10000 and activate the MDR control. Follow the switch positions indicated in the following table and verify that the correct code is displayed. The code identifies the switch position in the most significant digit and its data value is the least significant digit for most significant switch codes of 1, 2, 3 and 4. The display indicates the value on the MSB thumbwheel switch for values 5-9 and terminates this portion of the test when a 0 is present. Set switches as tabulated in Table V and observe correct codes. During the second portion of this test, the front panel display is tested. To activate this portion of this test, set a 0 in the most significant digit of the thumbwheel switches. The CPU outputs in sequence, the digits FF, EE, ..., 11, 00 to the display. Observe this sequence to assure that each digit is properly presented. This test sequence will identify hardware errors which occur on output to the display, that is a display of a different sense than that

TABLE V

SWITCH CODES

Switch	Display
10000	10
10007	17
10008	18
20008	20
20078	27
20088	28
30088	30
30788	37
30888	38
40888	40
47888	47
48888	48
78888	70
88888	80

output on a segment of the display being inoperative. Note especially the FF and 00 display which will identify output errors. If the FF (all bits on) display is not presented correctly, then the bit which is causing the problem is readily identified. Similarly for 00, all bits should be off. If a bit is being displayed as other than off, the digit display will be other than 0. See Table IV to isolate bit errors. Upon completion of this test, the self-test procedure immediately initiates the memory test sequence.

Memory Tests (F4, F5)

In these tests, processor memory will be examined. The first test assumes functionality of the processor Random Access Memory (RAM). During this test (F4), each location in RAM is examined. First, a binary word is written into the memory location; then, it is read and compared with the word written. If the comparison is not exact, the test fails and the memory segment which failed is displayed. Each memory location is tested with all possible combination of bits. Upon completion of the RAM test, a Read-Only Memory (ROM) test is initiated (F5). Each location in memory is added to form a checksum which is displayed on the front panel. If the checksum has changed since the processor was last programmed, memory error is identified. This is an operator comparison.

Memory testing is automatically initiated upon completion of the front panel tests and requires approximately 30 seconds to complete.

Display F4 identifies that the processor is in RAM test and F5 indicates ROM test. Failures will be noted by a display during RAM test of the address of the faulty memory segment, and during ROM test by noting that the checksum differs from previously established values.

FLIGHT

When the processor is a flight configuration, that is, it is not conducting self-test, there are three software defined modes or states which are present. These states are determined by operator selection of IDLE, RUN or HALT.

Idle

The IDLE state is used for operator specification of the processing configuration and occurs prior to data processing. During this state, which is entered upon reset, the processor reads data from the front panel pertinent to input and output units as well as angle selection data and any other processing information entered through the front panel thumbwheels. During this state the processor also accepts data from the aircraft pcm data and decodes

it for setup of processing parameters. The IDLE state must be reentered for the flight configuration to be changed. From a RUN state this is accomplished either by depressing IDLE, HALT or RESET. The processor will not enter the RUN state until all configuration variables are defined by the operator.

Operator input of certain processing parameters and modification of the internal aircraft flight parameter table is accomplished through the front panel thumbwheels. The most significant digit defines an operation code according to Table VI. In order to enter the parameter value, the proper opcode is selected and the parameter value set on the thumbwheels. After the data has been set up, the MDR switch is set to indicate valid data is ready for input. The processor will accept the input displaying the operation code and will reset the MDR flag. This operation will change the internal data table.

This mode of data entry is also used to provide for specification of the memory location, from which data are displayed. Memory locations 0 - 19999 (decimal) are determined by the thumbwheel switch input. Memory locations are identified from the software assembler listing and converted to decimal from the hexidecimal format. Entry of the decimal value on the thumbwheel switches and

TABLE VI

FRONT PANEL OP CODES

Op Code	Action
0	Display Address Selection 0-9999
1	Display Address Selection 10000-19999
2	Radar Altitude Set: Op 10^3 10^2 10^1 10^0 (Feet)
3	Roll Angle Set: Op S 10^1 10^0 10^{-1} S = + $(0)_1$-(1-9)
4	Drift Angle Set: Op S 10^1 10^0 10^{-1} S: + $(0)_1$-(1-9)
5	Pitch Angle Set: Op S 10^1 10^0 10^{-1} S: + $(0)_1$-(1-9)
6	Ground Speed Set: Op x 10^2 10^1 10^0 (Knots) X: Don't Care
7	Strip Chart Assignment: Op CH1 CH2 CH3 CH4
8	Initial Time-Index Set: Op 10^3 10^2 10^1 10^0
9	Date Set: Op MM YY
	Note: Op Codes 8&9 During Run Sequence Are Inoperative

selection of MDR causes the address to be saved by the processor. Then, the data in the specified memory location is output to the hexidecimal display.

Run

Once the processor has been programmed for flight processing, the RUN state may be initiated. In order to initiate this state, the RUN switch is set. The processor immediately begins processing data if a proper configuration has been specified. Error codes are displayed if this is not the case or if flight parameters cause processing limits to be exceeded. A feature of the processor system is the automatic alignment of the scattering coefficients as a function of angle for a single ground cell. Consequently, data from ground cells are incomplete until the last coefficient is determined.

During the RUN mode, data are processed according to the configuration specified by the operator.

Halt

The RUN mode can be orderly terminated by setting the HALT switch. Under this control an orderly termination sequence is enabled and the processor returns to the IDLE state. The IDLE state can also be entered if IDLE is depressed and RESET will cause an immediate cessation of processing and reinitialization of the software.

ANALOG SUBSYSTEM

The analog subsystem of the RTICS consists of an analog sign-sense network (Assembly A-1) and an analog spectral sampling network (Assembly A-2). Both assemblies, A-1 and A-2, are constructed on 16.5 cm x 25.4 cm (6.5"x 10") circuit boards and are shown in Figure 2. As observed in Figure 2, the majority of the discrete components are assembled on 16-pin component carrier modules which plug into socket pins placed in the board. Interconnection between the circuit modules is made by wire wrap on the back side of the board.

Each component on both A-1 and A-2 is identified on the corresponding schematic diagram by a reference number and element value. The location of any component may be found by referring to the component reference index which gives the module number, identifying the module location on the board and a second number which identifies the component position within the module. The numbering scheme for A-1 and A-2 is from left to right and from bottom to top as shown on the corresponding assembly diagrams.

The frequency compensation capacitors for the LM301 operational amplifiers and the power supply decoupling capacitors are not numbered since they are easily identified on the circuit boards and in the schematic and assembly diagrams.

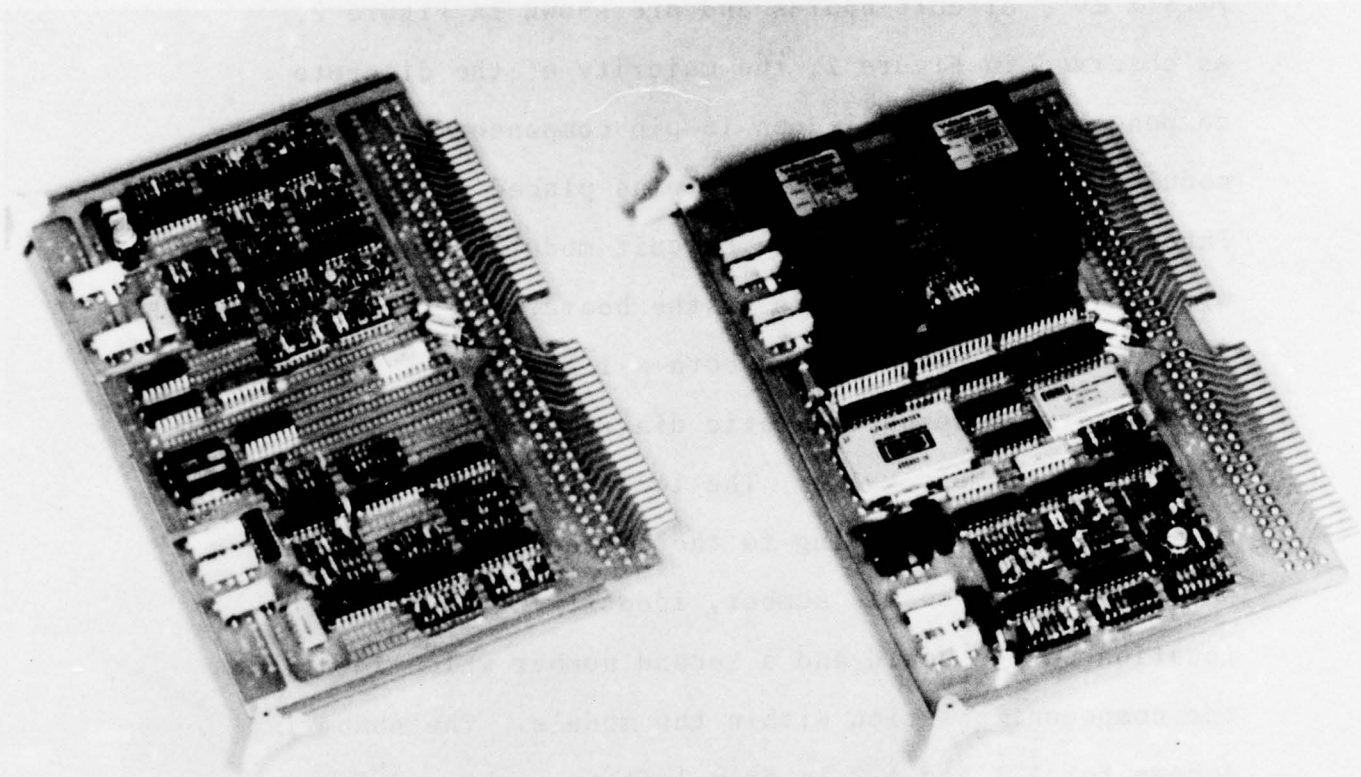


Figure 2. Analog Sign-Sense and Spectral Sampling Networks

ANALOG SIGN-SENSE NETWORK

The analog sign-sense network, Assembly A-1, performs quadrature signal processing functions on the Sine (SIN) and Cosine (COS) radar output signals to yield a single output signal which contains the unfolded fore and aft Doppler frequency spectra. The unfolding operation is accomplished by mixing the input SIN and COS signals with separate 20 KHz square wave signals which are themselves in phase quadrature. Prior to the mixing of the SIN and COS channels with the 20 KHz quadrature signals, the input signals are low-pass filtered in order to remove any out of band noise. The filter has a sixth order Butterworth response with a 15 KHz cutoff frequency. Following the mixing operation, the sum and difference of the resulting signals are performed. The sum and difference signals each contain the unfolded Doppler spectra but have the relative positions of the fore and aft data reversed. The selected sign-sensed output has the fore and aft data separated in frequency such that the fore data are above the 20 KHz carrier while the aft data are below the carrier in frequency.

In order to assure proper amplitude balance between the SIN and COS channels, the sum and difference signals are used to generate an AGC voltage which controls the gain of the SIN channel of the network. The AGC voltage

is obtained by multiplying the sum and difference signals together and low-pass filtering the product. The filtered signal amplitude is proportional to the amplitude difference between the SIN and COS channels. A reference voltage is added to the filtered signal which provides for setting the AGC level to an optimum range such that the error voltage is zero for balanced SIN and COS inputs.

In addition to the basic sign-sense processing functions, the sign-sense network also provides a pair of quadrature self-test signals which allows for real-time, in-flight verification of the entire analog front end. The input to the SIN and COS channels are switched from the radar signals to the internal self-test signals upon command from the digital processor CPU.

There are five potentiometer adjustments provided on board A-1 to assure optimum performance of the sign-sense network. Three of the adjustments are required to control the linearity and DC offset of the analog multiplier in the AGC loop. A fourth adjustment in the AGC loop sets the loop reference voltage such that when the SIN and COS channels are matched, the loop error voltage is zero. The fifth adjustment zeros the output DC level of the variable gain amplifier in the AGC channel.

The potentiometers, identified as R(1) through R(5), are located along the top edge of board A-1 and are

numbered from left to right looking at the component side of the board. Test points are located in the top center portion of the board and are also numbered left to right looking at the component side. The procedure for adjusting each of the potentiometers is given in Table VII, Board Alignment and Calibration Procedure, Assembly A-1.

Sign-Sense Input and Low-pass Filters

Input signals to the sign-sense network are software selectable to be either the radar SIN and COS signals or internally generated quadrature self-test signals. Input selection is accomplished by FET switch ZK1. The self-test command signal, the MSB of the first VCO frequency control data word, is held in a "D" flip flop (ZJ2) which in turn controls the input selection switch. If the self-test command is TRUE (a high TTL level), the inputs to the sign-sense network are the self-test signals.

Following the input selection switch are parallel SIN and COS signal processing channels. Each channel consists of an input buffer amplifier followed by a three stage low-pass filter. The buffer amplifiers (ZB1 and ZV1) are LM301 operational amplifiers connected in a unity gain configuration with an input impedance set at 10 KΩ.

The filters which follow are Voltage Controlled Voltage Source (VCVS) active low-pass filters. The COS

Table VII. - Board Alignment and Calibration Procedure - Assembly A-1

The following adjustments are to be made with the processor in the self-test mode of operation.

Step 1 With a short clip lead, ground pin 9 of ZE7. Connect a scope probe at Test Point 1 and observe the output waveform. Adjust potentiometer R(1) such that a minimum AC signal component is present.

Step 2 Repeat step 1 except, ground pin 10 of ZE7 and adjust R(2) for minimum AC signal component at Test Point 1.

Step 3 Ground both pins 9 and 10 of ZE7 and adjust R(3) for zero DC offset at Test Point 1.

Step 4 Connect the scope probe to ZV6 Pin 6. Observe an approximate 1 volt level, 20 KHz suppressed carrier modulated waveform. (The modulation waveform is the 1.25 KHz square wave self-test signal). Adjust R(5) for minimum DC level at ZV6 Pin 6.

Step 5 Connect a spectrum analyzer to the sign-sense output (Pin 6 of ZE1 or P2-8). Set the spectrum analyzer to a 20 KHz center frequency with a frequency scale and bandwidth setting such that the 1.25 KHz and 3.75 KHz harmonics of the self-test signal may be identified. Adjust R(4) for minimum 3.75 KHz harmonic content (23.75 KHz) in the sign-sense output.

channel filter is comprised of ZB2, ZB3 and ZB4. The SIN channel filter elements are ZV2, ZV3 and ZV4. As noted previously, the filters exhibit a sixth order Butterworth response characteristic with a cutoff frequency of 15 KHz.

Following the low-pass filter in each channel is an inverting amplifier whose output, along with the direct filter output, provides balanced input signals to the mixer stage of each channel.

Quadrature Reference Signal Generation

The 20 KHz quadrature square wave reference signals are generated on A-1 using TTL logic circuits. An 80 KHz crystal controlled oscillator (ZG1) provides a stable signal from which the 20 KHz signals are derived. The oscillator output is first divided by two by a "D" flip flop (ZJ2). The Q and $\overline{Q}$ outputs of the flip flop provide complementary 40 KHz clock signals which each drive a divide-by-two circuit. Since the clock signals are 180 degrees out of phase, the 20 KHz signals out of the divide-by-two-circuit will be 90 degrees out of phase. To guarantee that the SIN channel reference signal always lags the COS reference signal, a 2-input NAND gate is used to generate a feedback control signal which allows the SIN channel divide-by-two circuit to toggle only after the COS circuit.

Frequency Offset Mixers

The mixer circuit in both the SIN and COS channel is implemented by means of a TTL compatible FET analog switch. The quadrature complementary 20 KHz reference signals described above drive the switch control inputs which serve as the local oscillator input.

The switching action of the mixer is to alternately select the direct and inverted filter outputs at a 20 KHz rate. The result is that the radar signal is multiplied by a unit amplitude 20 KHz reference.

The mixer output signal in the COS channel is buffered by a unity gain, non-inverting op amp (ZB6). In the SIN channel, the mixer output is fed to a variable gain amplifier (ZW4) which provides for automatic adjustment of the SIN channel amplitude such that the SIN and COS channels are matched. Since the variable gain amplifier exhibits a nonzero DC output level, an offset adjustment is provided by R(4) and op amp ZV6.

Sum and Difference Network

Addition and subtraction of the COS and SIN channel (i.e., COS + SIN and COS - SIN) are implemented by operational amplifiers ZE2, ZE3, and ZD4. A unity gain buffer (ZE1) provides the sign-sense output signal which is routed to the spectral sampling network.

AGC Loop

Both the sum and difference signals are implemented in order that they be available for generating the signal which automatically controls the gain of the SIN channel. It is the difference signal which provides the actual sign-sense output.

To generate the AGC voltage, the sum and difference signals are multiplied together by means of a four quadrant analog multiplier (ZE7). The DC component of this product is proportional to the amplitude difference between the COS and SIN channels. This signal is low-pass filtered, added to an offset reference voltage and applied to the AGC input of the SIN channel variable gain amplifier.

Self-Test Signal Generation

As previously noted, a pair of quadrature square wave signals at 1.25 KHz are provided as part of the sign-sense network which are selected as the sign-sense input signals in the SELF-TEST mode of operation. These signals are generated from the 80 KHz crystal controlled oscillator, as are the 20 KHz reference signals.

Similar to the reference signal generation, the SELF-TEST circuit uses TTL flip flops, a decade counter and TTL NAND gate to generate quadrature square wave signals.

The TTL level signals are buffered by diode, resistor and transistor circuits (refer to schematic diagram) which are followed by LM301 op amps to convert the complementary TTL signals to balanced analog signals.

The op amp outputs are connected to the FET input selection switch through 330 K resistors which provide the correct signal levels to the sign-sense network input.

Radar Failure Detection

In addition to the self-test function which monitors the operation of the sign-sense network, a radar failure detection circuit is also provided as a performance monitoring function.

The radar failure detection circuit consists of two voltage comparitors (implemented with LM301 op amps ZS5 and ZS6) which operate on the AGC voltage to detect the presence of a gross unbalance between the SIN and COS channels or excessive noise in either channel. Two voltage comparitors are required since a large positive AGC voltage signifies loss of the COS channel, whereas a large negative voltage implies loss of the SIN channel.

In actual operation, the circuit does not detect loss of the COS channel unless excessive noise appears in place of the COS signal. The reason for this behavior is quite reasonable since when the COS channel input is zero

volts, the AGC voltage attempts to reduce the SIN channel signal level to zero also. As the SIN channel signal tends to be reduced to a very low level, the resulting AGC voltage is also small, so that in the steady state condition, the AGC voltage level returns quickly to a level within the normal operating range.

When a radar failure is detected, the event is communicated to the CPU through bits five and six of the upper byte of the digital output data word. The processing software recognizes the failure mode and lights the RADAR FAIL indicator on the front panel.

ANALOG SPECTRAL SAMPLING NETWORK

The analog spectral sampling network operates on the unfolded or sign-sensed Doppler spectra to measure the power returned from a desired incident angle. Angle selection is accomplished by mixing the input sign-sensed signal with the output of a voltage controlled oscillator (VCO) whose frequency is determined by a 12-bit digital word written to the digital-to-analog interface from the CPU.

The VCO frequency is selected such that the desired Doppler frequency band is shifted to zero hertz center frequency. The resulting baseband signal is then low-pass filtered, full wave rectified, integrated and

converted to a 12-bit digital word which is then read by the processor CPU.

The details of the circuit functions are described as follows. The CPU initiates the spectral sampling operation by writing two 8-bit control words to the spectral sampling network digital interface. This interface consists of four 8-bit data registers (Intel 8212's). Two registers accept and hold data from the CPU via the tri-state data bus; the remaining two hold the analog-to-digital (A/D) converter output and system status bits, which are placed onto the bi-directional data bus upon command from the CPU.

The first control word written to the interface contains a mode control bit and the four most significant bits (MSB's) of the 12-bit VCO control word. The MSB of this data word is the mode control bit. If the bit is "1", the analog system is placed in the SELF-TEST mode; a "0" commands the normal operate mode.

The remaining eight bits of the VCO control word are written to the second input register of the interface by a second write instruction from the CPU. Upon recognizing this instruction, the spectral sampling integrator (ZE3) is dumped and is then allowed to integrate for approximately 100 milliseconds. The dump and integrate

functions are implemented by two one-shots, ZB7 and ZE7, respectively, which control FET switches ZF1 and ZF2 (see schematic diagram).

At the end of the 100 msec integration interval the CPU writes a "start convert" command to the A/D convertor. The CPU tests bits seven and eight of the most significant data byte (the 8212 which contains the four MSB's of the integrator output word) to determine the status of the dump and integrate one-shots. An "end of convert" signal controls the CPU READY line to allow the data to be transferred to the CPU at the end of the data cycle. The CPU reads the output interface in two separate instructions. The first read accepts the status bits and four MSB's of the data. The second read accepts the remaining eight bits of the data word.

There are two possible sources of sign-sensed data for input to the spectral sampling network. In addition to the direct output of the sign-sense network, Assembly A-1, recorded sign-sense data may be input via the back panel connector. A switch in the upper left hand corner of A-2 controls the input source to the spectral sampling circuit. In the UP position the switch selects the direct sign-sense network output, whereas external sign-sense data may be processed by placing the switch in the DOWN position.

There are nine adjustments provided on A-2 to assure optimum performance of the spectral sampling functions. R(1), a 50 KΩ potentiometer is a carrier suppression adjustment for the input mixer ZB1. R(2) adjusts the integrator output level to zero volts for zero input signal.

R(3) is a 20 KΩ potentiometer which is used to select the desired integration time interval. R(4) and R(5) set the VCO range and zero reference.

R(5), R(7), R(8) and R(9) provide for optimum performance of the Wavetek 120-021 voltage controlled oscillator and the 120-022 sine shaper module. The proper procedure for adjusting potentiometers R(1)-R(9) is given in Table VIII.

Voltage Controlled Oscillator

The voltage controlled oscillator for the spectral sampling network is comprised of a Wavetek 120-021 generator module and a Wavetek 120-022 sine shaper module. The frequency range of the VCO is set for 10 to 35 KHz corresponding to digital inputs from FFF_{16} to 0_{16}, respectively. The digital control word is converted to an analog control voltage by a Burr-Brown DAC-85 D/A converter.

Op amps ZE1 and ZE2 buffer this analog voltage and along with trimpots R(4) and R(5) allow for independent

Table VIII. Control Adjustment and Calibration Procedure, Assembly A-2

The following adjustments are to be performed with the scratch pad memory (ssembly A-6) inserted in circuit board location 4.

Step 1. Enter the following program into the scratch pad memory via the front panel interface.

Location (HEX)	Instruction (HEX)
0000	3E
0001	FF
0002	D3
0003	OC
0004	D3
0005	OB
0006	76

Connect a frequency counter to test point 11. Execute the program. Adjust R(5) for 10 KHz output at test point 11.

Step 2. Modify the above program as follows:

Location (HEX)	Instruction (HEX)
0001	00

Execute the program. Adjust R(4) for 35 KHz output at test point 11.

Step 3. Repeat steps 1 and 2 until adjustments converge.

Step 4. Connect an oscilloscope to test point 10. Adjust horizontal and vertical scales for a convenient display. Adjust R(7) for zero DC offset at test point 10.

Step 5. Connect a spectrum analyzer to test point 9. Adjust center frequency and scan width such that VCO fundamental and first and second harmonics can be observed. Adjust R(6), R(8), and R(9) for optimum harmonic suppression.

Step 6. Modify the program in Step 1 as follows:

Location (HEX)	Instruction (HEX)
0001	0S

Execute the program. Connect a 0.5 Volt peak-to-peak 10 KHz signal to the external sign-sense input, move the sign-sense input selector switch to the DOWN position. Connect the spectrum analyzer probe to ZB2 pin 6. Adjust the analyzer center frequency and scan width to display the carrier and upper and lower sidebands of the mixer output. Adjust R(1) for maximum carrier suppression.

Step 7. Replace Assemblies A-4 and A-6 to their proper locations. Operate the processor in the normal run mode. Connect an oscilloscope to pin 6 of ZE7. Adjust R(3) for an output pulse width of 100 milliseconds at pin 6.

adjustment of VCO range and free run (0 volts - FFF_{16}) frequency.

Input Mixer

The input mixer for the spectral sampling network is a Motorola MC1596G balanced mixer integrated circuit. This mixer exhibits excellent linearity and carrier suppression characteristics which may be optimized by adjusting trimpot R(1) (see Table VIII).

Low-Pass Filter and Signal Integration

The Doppler frequency selection filter is of similar design to the sign-sense input filters. That is, it is a three stage VCVS active filter which has a sixth order Butterworth response. Two sets of component modules have been provided for the low-pass filter which yield cutoff frequencies of 100 and 200 Hz. Since the filters are of low-pass design, the effective Doppler bandwidth is twice the low frequency cutoff, or 200 and 400 Hz, respectively.

The output of the filter is corrected for DC offset error, full wave rectified, inverted and applied to the input of the integrator. The integrator circuit consists of FET switches ZF2 and ZF3 and op amp ZE4.

At the start of the integration period, the integration capacitor C13 is dumped by FET Switch ZF3. Switch ZF2 then opens up the integrator input for a period of 100 msec. At the end of the 100 msec interval the CPU issues a "start convert" command to the A/D converter which converts the integrator output voltage to a 12-bit digital word. The integration voltage range is 0 to 10 volts.

CENTRAL PROCESSOR AND MEMORY SYSTEM

The central processing unit (CPU) and the associated memory system forms the heart of the RTICS system. The following sections describe in detail the design and implementation of the RTICS special purpose computer which is built around the Intel 8080 microprocessor.

The Intel 8080 Microprocessor

The majority of the computational and control operations of the RTICS system take place in or originate from the Intel 8080 microprocessor chip. The 8080 is an NMOS large scale integrated circuit housed in a 40-pin dual in-line package (see Figure 3a). Figure 3b illustrates the functional architecture of the 8080. A 16-bit address bus and an 8-bit data bus are directly accessible so that up to 64K (65, 536) bytes of memory

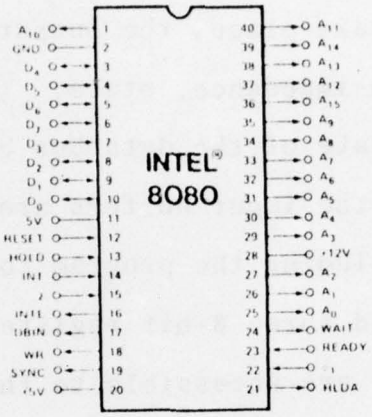


Fig. 3a. 8080 Pin-out

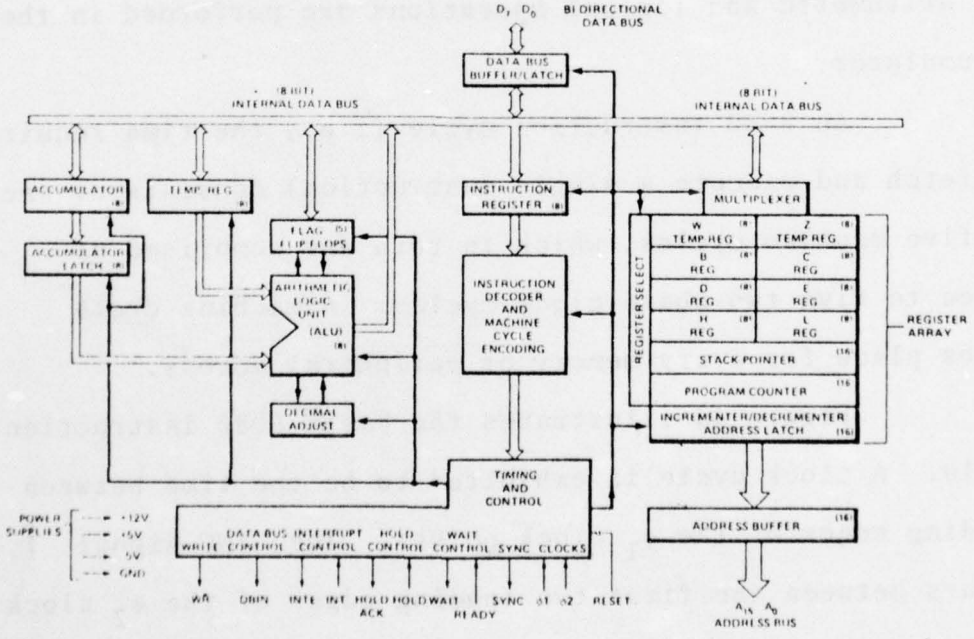


Fig. 3b. Functional Architecture of the 8080

or input data can be directly addressed. The data bus is bi-directional; that is, each data line is buffered in either direction (input or output) by a three-state buffer. If data input is to take place, the output buffer is placed in the third, or high-impedance, state. The control line DBIN indicates the state of the data bus buffers and is TRUE (+5 Volts) when the input buffers are enabled. Five 16-bit registers, including the program counter (PC), stack pointer (SP) and three 8-bit register pairs (B and C, D and E, H and L), are accessible to the user via instructions. The six registers of the pairs are addressable either separately or as pairs. The Arithmetic and Logical Unit contains an 8-bit accumulation and a 5-bit flag resistor. All arithmetic and logical operations are performed in the accumulator.

An 8080 instruction cycle (i.e., the time required to fetch and execute a single instruction) consists of one to five machine cycles, which in turn are comprised of three to five two-phase clock cycles. A machine cycle takes place for every memory or peripheral access.

Figure 4a illustrates the basic 8080 instruction cycle. A clock cycle is exhibited to be the time between leading edges of the ϕ_1 clock pulses. The SYNC signal occurs between the first two leading edges of the ϕ_2 clock

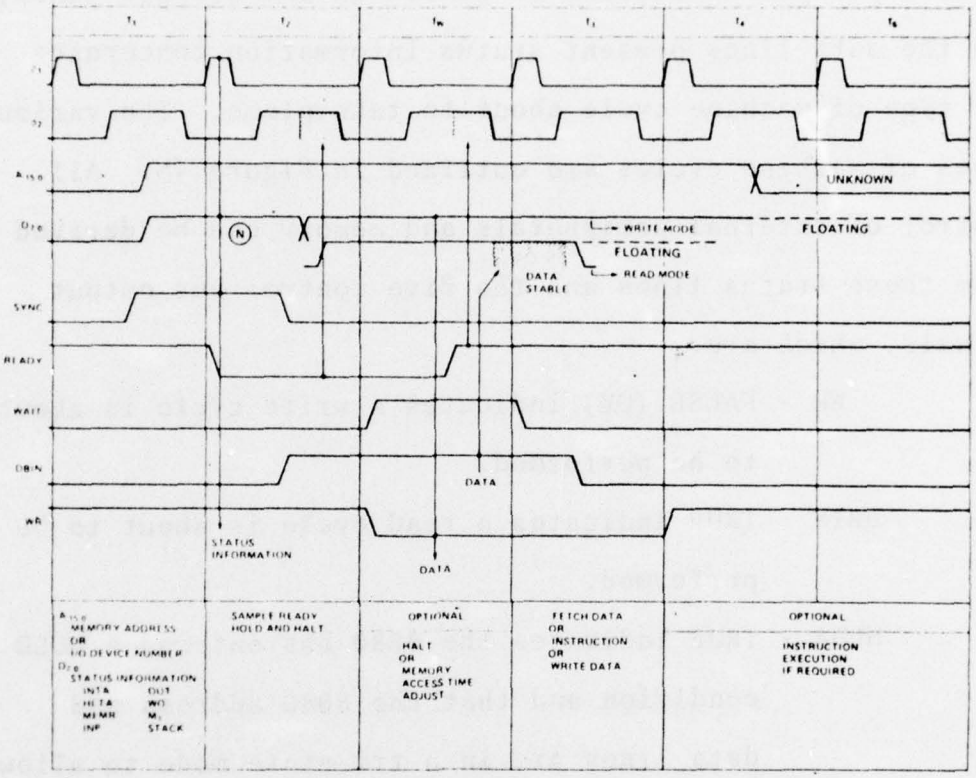


Fig. 4a. The 8080 Instruction Cycle

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	(1) INSTRUCTION FETCH	(2) MEMORY READ	(3) MEMORY WRITE	(4) STACK READ	(5) STACK WRITE	(6) INPUT READ	(7) OUTPUT WRITE	(8) INTERRUPT ACKNOWLEDGE	(9) HALT ACKNOWLEDGE	(10) INTERRUPT ACKNOWLEDGE WHILE HALT
		(N) STATUS WORD									
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	WO	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

Fig. 4b. 8080 Machine Cycles

of every machine cycle. During a SYNC pulse, either the PC or a peripheral address is placed on the address lines, and the data lines present status information concerning the type of machine cycle about to take place. The various types of machine cycles are outlined in Figure 4b. All control of external peripherals and memory can be derived from these status lines and the five control bus output signals, which are:

WR - FALSE (0V) indicates a write cycle is about to be performed.

DBIN - TRUE indicates a read cycle is about to be performed.

HLDA - TRUE indicates the 8080 has entered a HOLD condition and that the 8080 address and data lines are in a tri-state mode to allow direct memory access type operations.

INTE - TRUE indicates that a vectored interrupt can be initiated by a peripheral by placing a TRUE signal on the interrupt (INT) line.

Processor Program flow can be altered by the four control bus input signals in the following manner:

RESET - TRUE restores the 8080 PC to zero. Program execution begins at memory location zero following a RESET.

READY - FALSE causes the 8080 to enter a wait cycle, which suspends further processing until READY becomes TRUE again. This allows slow access devices to delay processing until valid data is available.

HOLD - TRUE forces the 8080 to tri-state the data and address busses after the current instruction's use of the busses is over.

INT - TRUE during INTE TRUE causes the processor to accept a vectored interrupt after the current instruction is executed.

The 8080 can perform 78 different operations, with each instruction requiring from one to three 8-bit bytes of memory. Instruction execution and program flow can best be illustrated by the state flowchart of Figure 5. After a RESET or an Interrupt, the first machine cycle executed is an instruction fetch cycle. After checking the READY and HLTA conditions (execution of a HALT instruction suspends processor operation until an Interrupt or RESET), and if neither condition is TRUE, setting a HLDA flag if HOLD is TRUE, the first byte of the instruction is fetched from memory. This byte is decoded and any execution possible performed. If the decoding indicates the instruction is more than one byte long, a memory read

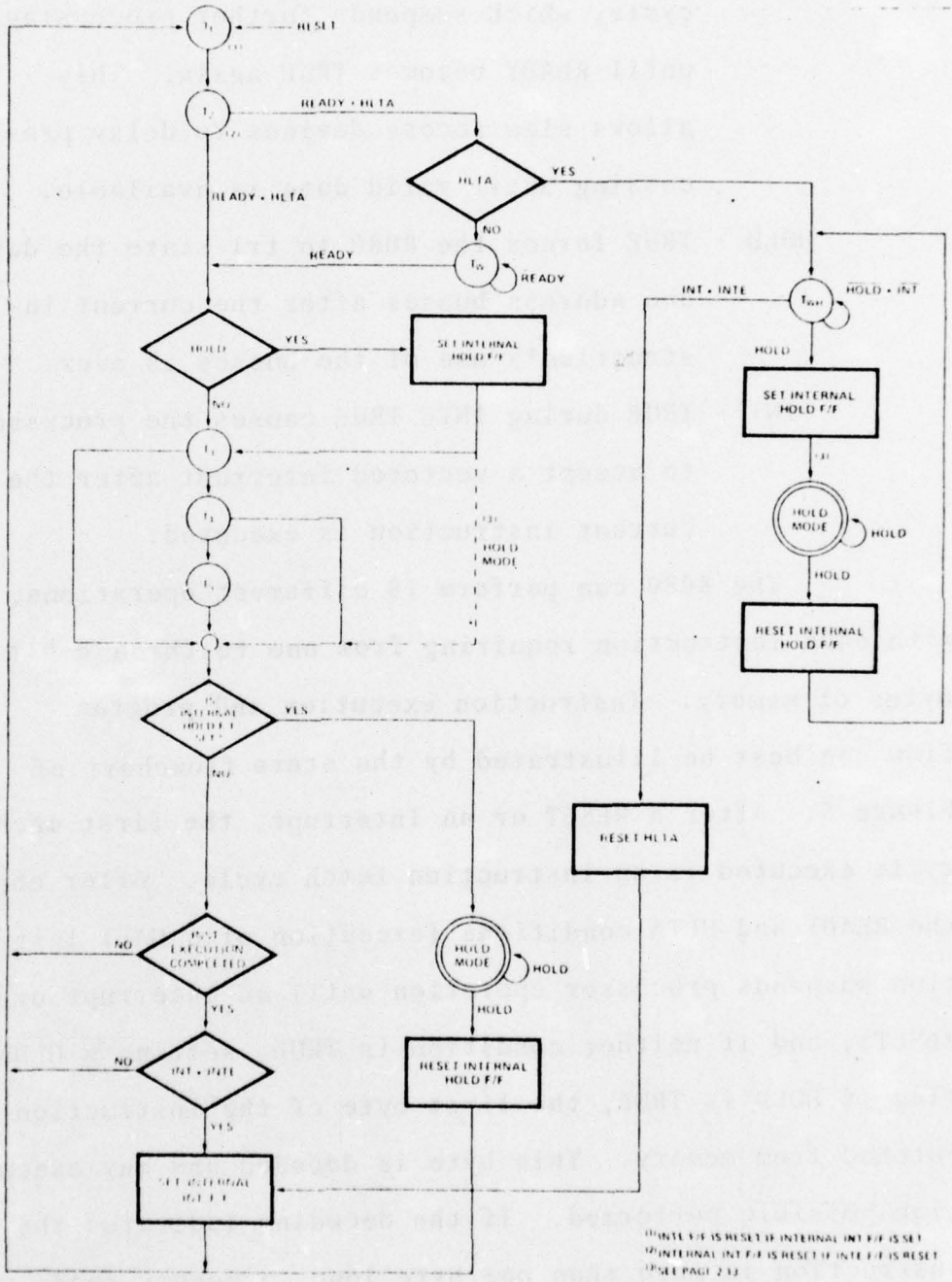


Fig. 5. 8080 State Flow Chart

cycle is initiated to fetch the next byte. This continues until the instruction execution is completed, when a new fetch cycle is initiated for the next instruction.

The 8080 instruction set consists of 78 possible instructions. An often used figure of merit in mini- and microcomputer work is the add cycle time, or the time required to fetch and execute an addition to the accumulator. For the 8080, the add cycle time is two microseconds, as compared to a range of 0.5 to 1.5 microseconds which covers most minicomputers.

CENTRAL PROCESSOR DESIGN

The design of a central processing unit incorporating the 8080 is for the most part a task of interfacing the various peripherals and storage with the three busses: address, data and control. The sequential enabling and disabling of the devices onto the busses must occur within various time limitations and bus conflicts avoided. A bus conflict is an attempt by more than one device to bring data onto a bus at the same time.

A functional breakdown of the RTICS CPU is presented in Figure 6. In the figure, bus paths are denoted by wide strips, with a number to indicate the width of the bus. Detailed schematics of the CPU are presented in Appendix A.

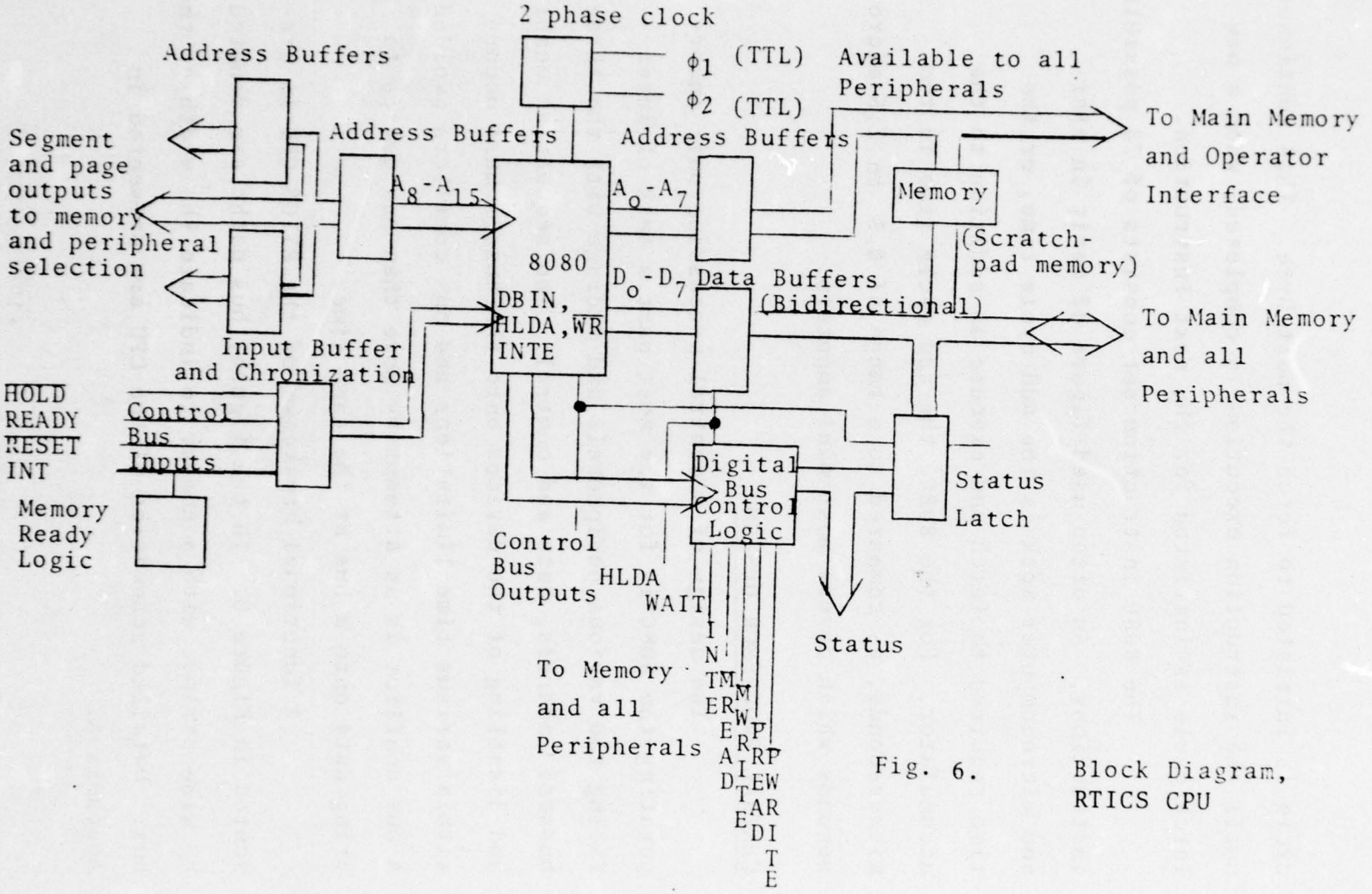


Fig. 6. Block Diagram, RTICS CPU

The CPU, along with the PI/O unit, is constructed on a 6.5" x 10" wire-wrapped circuit board designated assembly A-3 (shown in Figure 7). Two 44-pin edge connectors provide a "common bus" to all external devices with the address, data, control, status and other CPU signals available.

The address, data and control output busses are buffered outside the 8080 by high current (50MA SINK) drivers (ZL4, ZM4, ZL3 and ZM3) to provide the fan-out and noise immunity required in a bussed system. The Intel 8216 data bus drivers are bi-directional and tri-state.

The two-phase 2 MHz clocks (ZG1), ϕ_1 and ϕ_2, are available at TTL levels to external devices as well as the NMOS levels (0 to $\pm$ 12 volts) input to the 8080.

In order to simplify memory and peripheral addressing, the address lines A_8 - A_{13} are decoded into 16 lines through two three-to-eight line decoders (ZE4 and ZF4). In memory applications, the decoding of A_8 - A_{10} can be used to select eight "pages" of 256 bytes. Address lines A_{11} - A_{13} decoded provide selection between eight "segments" of eight pages each. Thus, the total addressability using the decoded address lines is eight segments of eight pages of 256 bytes each, or 8 x 8 x 256 = 16,384 bytes. The 256 byte page size allows use of the smaller memory chips available, and larger capacity RAM or ROM can be easily addressed as combinations of the pages and/or segments.

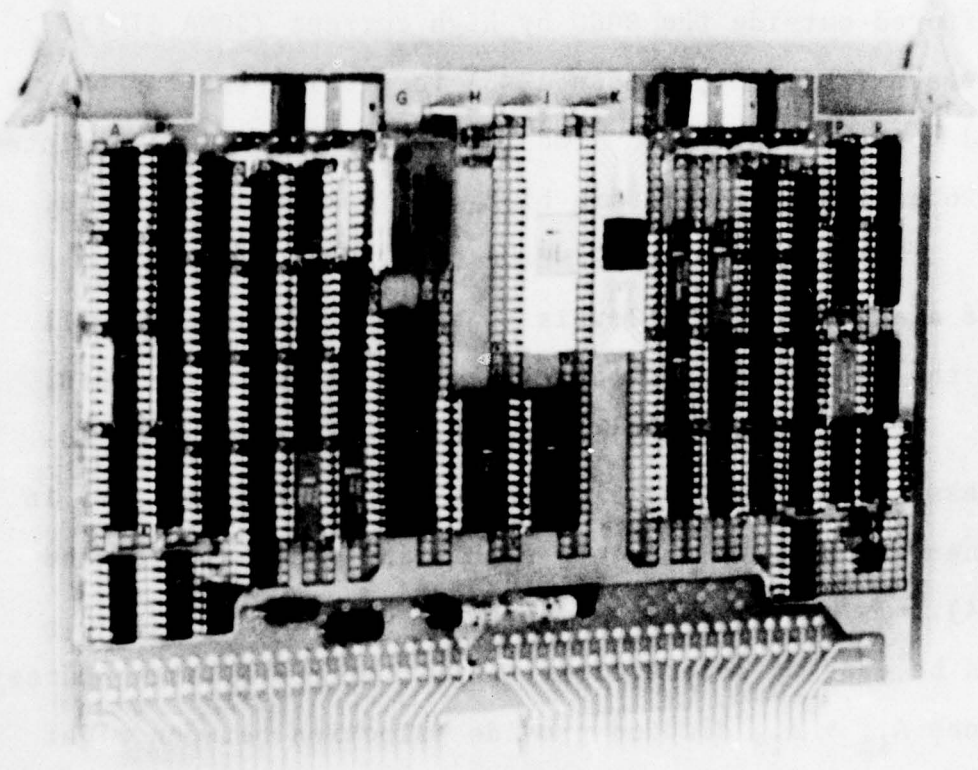


Figure 7. Central Processor Assembly

The decoded addresses also allow peripheral devices to be simply addressed. During IN or OUT instructions, which are the only 8080 instructions affecting peripherals, the address of the device, up to 256_{10}, is placed on address lines A_8 - A_{15}. Up to 64 input and output devices can be uniquely identified using one segment output ($\overline{S}_0$ through $\overline{S}_7$, the active FALSE decoding of A_{11} - A_{13}) and one page output ($\overline{P}_0$ through P_7, the active FALSE decoding of $\overline{A}_8$ - A_{10}) for each device. Since the input or output conditions are flagged by the status bits OUT and INP, one output device (a device which reads from the data bus) and one input device (a device which acts as a source of data) can be assigned to each of the 64 possible device codes.

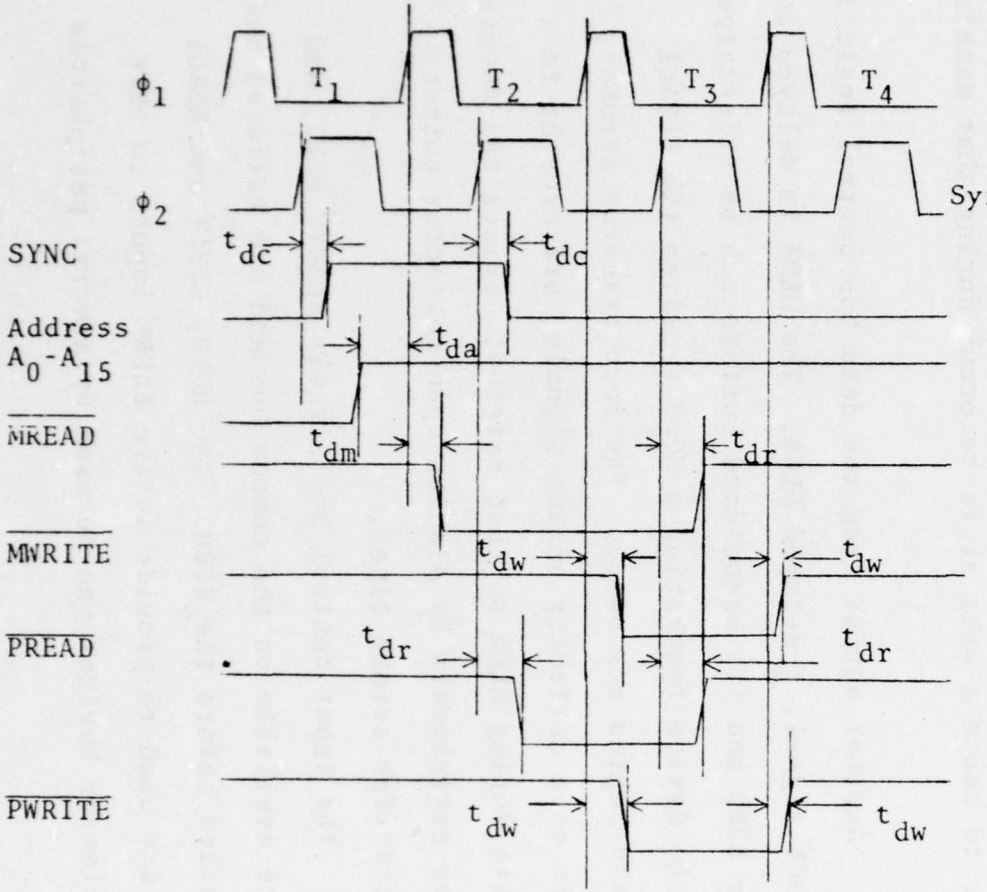
DATA BUS CONTROL

During the fetch and execution of each instruction, each machine cycle requires the exchange of data over the bi-directional bus so that either DBIN or $\overline{WR}$ become active during the third clock cycle of the machine cycle (see Figure 4b). At the same time, the status outputs indicate whether memory or a peripheral device is involved and whether the transfer is a read or write.

The data bus control logic accepts as inputs the status, DBIN, WR and HLDA. Four active FALSE outputs are available from the logic: $\overline{\text{MREAD}}$ (memory read), $\overline{\text{MWRITE}}$ (memory write), $\overline{\text{PREAD}}$ (peripheral read), and $\overline{\text{PWRITE}}$ (peripheral write). These signals are available to all peripherals and memory and allow simple interface with the common data bus. Figure 8 is a timing diagram of the four data bus control signals as they occur in a typical machine cycle. Also shown are the data stable (t_{ds}) times required. During t_{ds}, the data from the 8080 or the peripheral must remain constant; during a $\overline{\text{PWRITE}}$ or $\overline{\text{MWRITE}}$ is the time during which data may be latched into the device or memory.

The $\overline{\text{MREAD}}$ output indicates that data from the memory address on the address bus should be placed on the data bus and remain stable during the period indicated in the figure. An active $\overline{\text{MWRITE}}$ indicates that data to be placed in the memory address will be stable for a period around the rising edge of $\overline{\text{MWRITE}}$. The $\overline{\text{PREAD}}$ and $\overline{\text{PWRITE}}$ signals are quite similar except that the address should be interpreted as a peripheral device number.

Memory or devices which cannot accept source data within the setup times indicated must provide some type of READY line control to lengthen the transfer strobes. By taking the READY line FALSE during the second clock cycle



Symbol	Parameter	min nsec	max nsec
t_{dc}	SYNC output delay		120
t_{da}	Address delay		200
t_{dm}	Memory read transfer delay	80	120
t_{dr}	Read delay	25	155
t_{dw}	Write delay		135

Fig. 8. Transfer Strobe Timing

of the machine cycle, the processor is forced into a wait cycle until the READY line is TRUE again. The transfer strobes remain active during the wait states, then go TRUE to latch data into the 8080 or provide a latching edge of the peripheral. The timing diagrams for devices requiring one or two wait states are shown in Figure 9. Note that the READY line must be set up prior to the rising edge of ϕ_2 during the second clock cycle of a particular machine cycle in order to cause a wait state to occur during that machine cycle.

Another output from the data bus control logic is the HLDACK signal, a delayed HLDA. The HLDA is delayed so that the 8080 and its associated buffers can be tri-stated before the device requesting a HOLD receives the HLDACK signal and begins bus usage. The four transfer strobes, which are open collector output signals, are brought to a TRUE state during HLDA so that external devices can access memory or peripherals by placing open collector outputs on the transfer strobe lines.

The input control bus signals READY, HOLD, and RESET are available on the common bus and are buffered and synchronized before the 8080. The HOLD, RESET and READY signals are used to provide active FALSE inputs so that open collector devices can be used by several peripherals

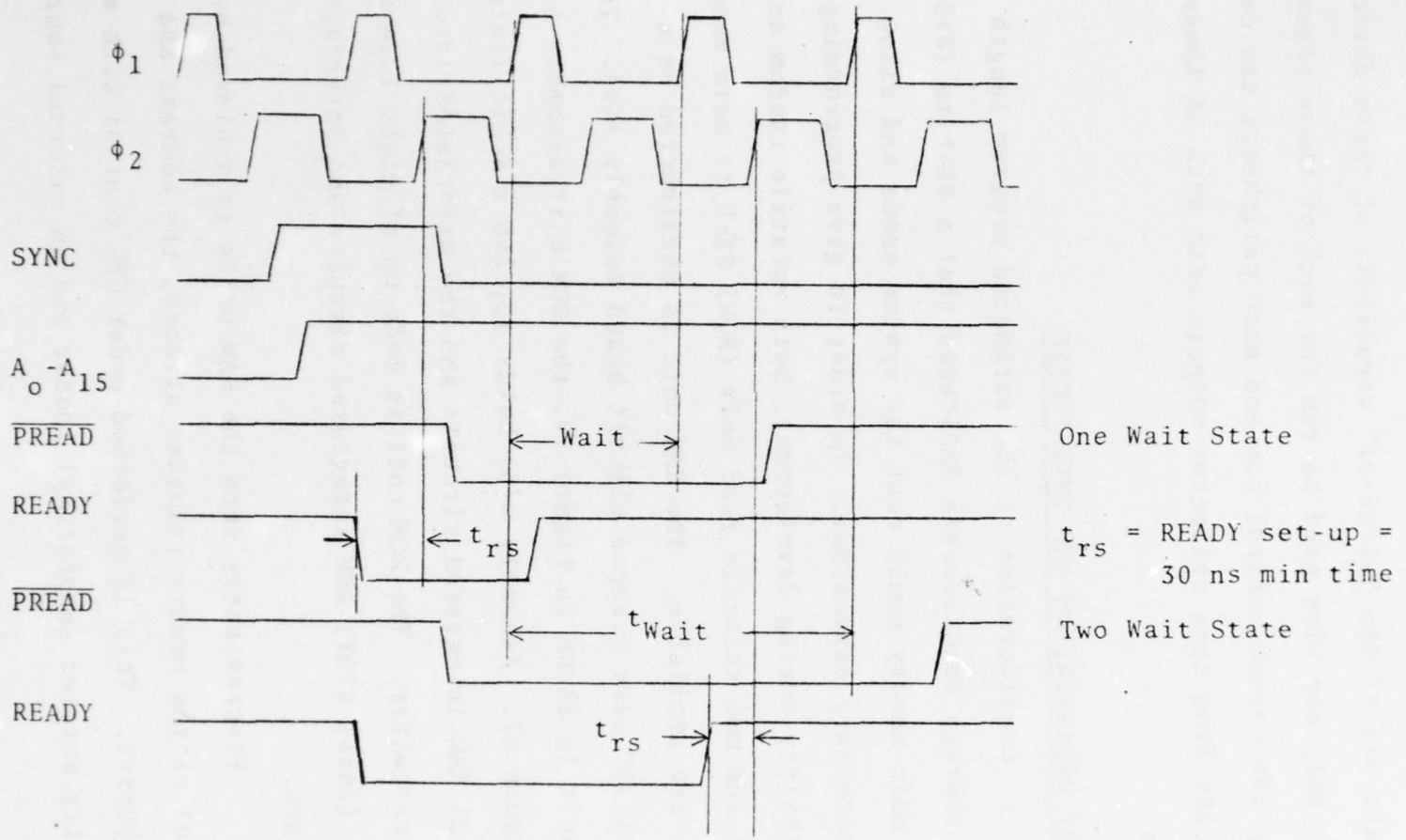


Fig. 9. Using the READY Line to Lengthen a Transfer Strobe

to make use of the "wired-or" capability of these devices. Thus, only one wire need be run for each of these signals along the common control bus and each peripheral can control the 8080 from open collector outputs onto each of these lines.

MEMORY ORGANIZATION AND INTERFACING

Consideration of the estimated program length and data storage requirements indicated that a 8K-byte (8192 x 8) main memory would meet the system needs and allow for any necessary expansions. In order to give programming flexibility during development, both volatile random access (RAM) and non-volatile read only (ROM) 8K-byte main memory units are available. The RAM unit is constructed on a 6.5" x 10" wire wrapped circuit board assembly A(6). The RAM unit is shown in Figure 10, the ROM unit assembly A(4) in Figure 11. Assembly A(6) holds 32, 256 x 4-bit (Intel 8111-2) RAM integrated circuits and the associated interface circuitry. The ROM unit is made up of eight 1024 x 8-bit (Intel 8708) ROM integrated circuits and interface hardware.

Program entry into the RAM units is achieved by control of the memory transfer strobes, the address and the data busses. This is performed under CPU control with a manually entered (bootstrap) loader and an external source

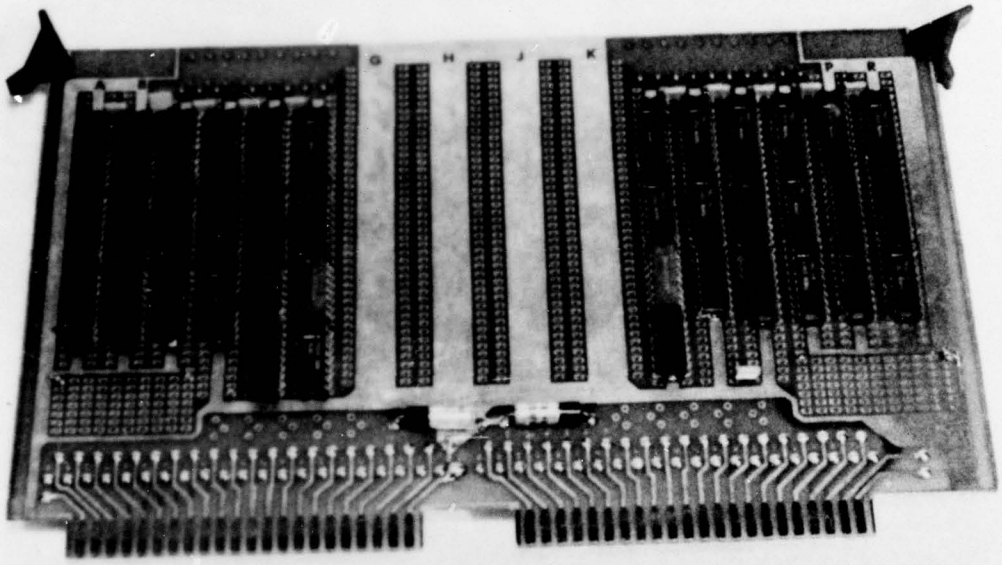


Figure 10. Random Access Memory Assembly

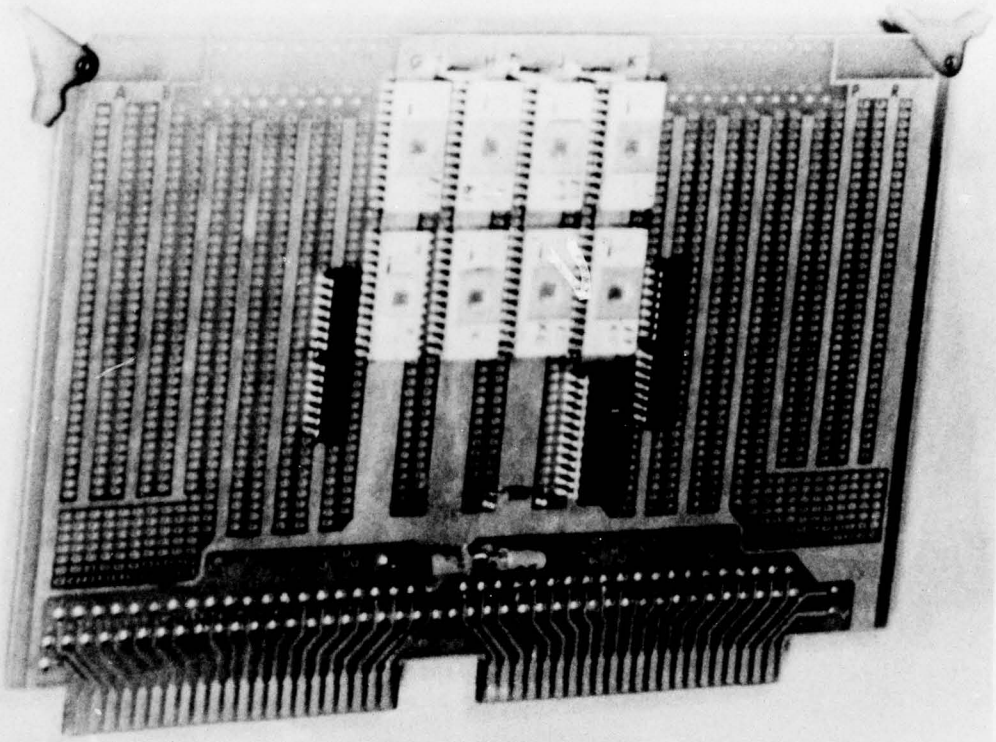


Figure 11. Read Only Memory Assembly

of data through the peripheral interface unit. The ROM circuits must be programmed outside the processor. The 8708 circuit is electrically programmable and is erasable under ultraviolet light.

Figures 12a and 12b illustrate the interfacing of the memory units to the common bus. The RAM unit is divided into two banks of 16 chips, each bank representing a 4096 x 4 block of memory. The Page and Segment lines from the CPU enable only one device from each bank for a given address. During an active $\overline{\text{MREAD}}$, the enabled chips' output buffers, which are tri-state, are enabled onto the memory data bus and the eight low order address bits select the data word to be read out. The bi-directional buffers are selected to place data onto the common data bus. Otherwise, the buffers are selected to bring data off the bus onto the memory data bus, the memory output buffers are disabled and the $\overline{\text{MWRITE}}$ line controls the active FALSE write input on the chips.

The ROM unit is quite similar to the random access board in operation. Since only read operations occur from the ROM board, a single 8-bit, three-state buffer (Intel 8212) is used to gate the addressed data onto the data bus during an active MREAD. The ROM chip selection is accomplished by using the segment lines and address bit ten (A_{10}). The A_{10} bit selects between the two ROM chips which make up the 2K segment being addressed.

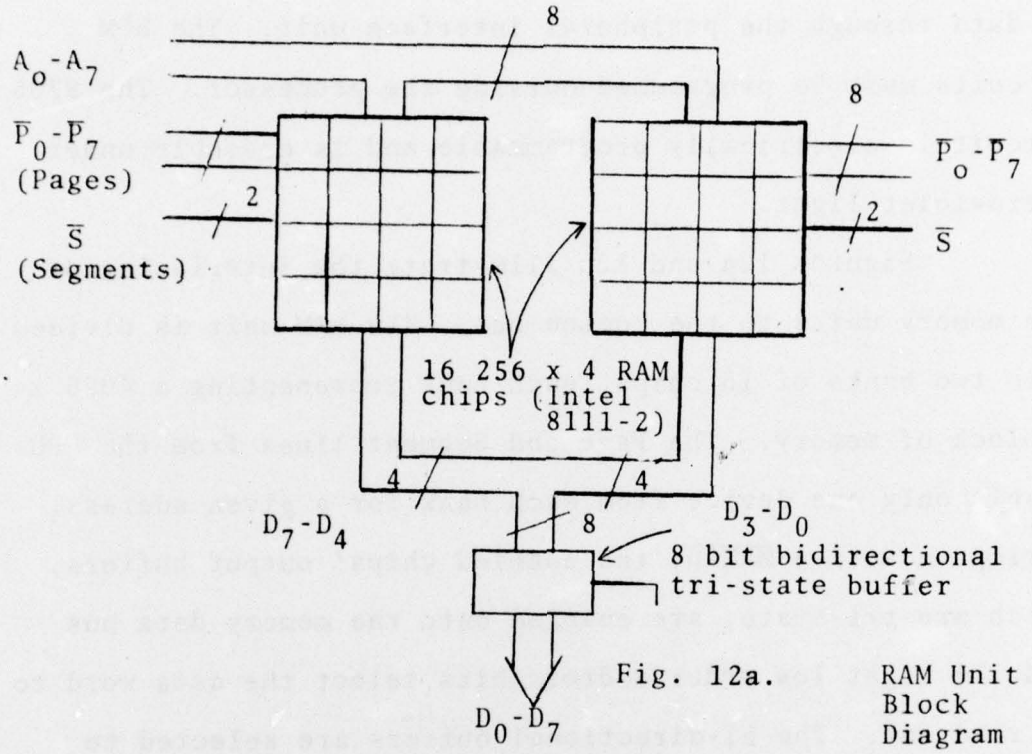


Fig. 12a. RAM Unit Block Diagram

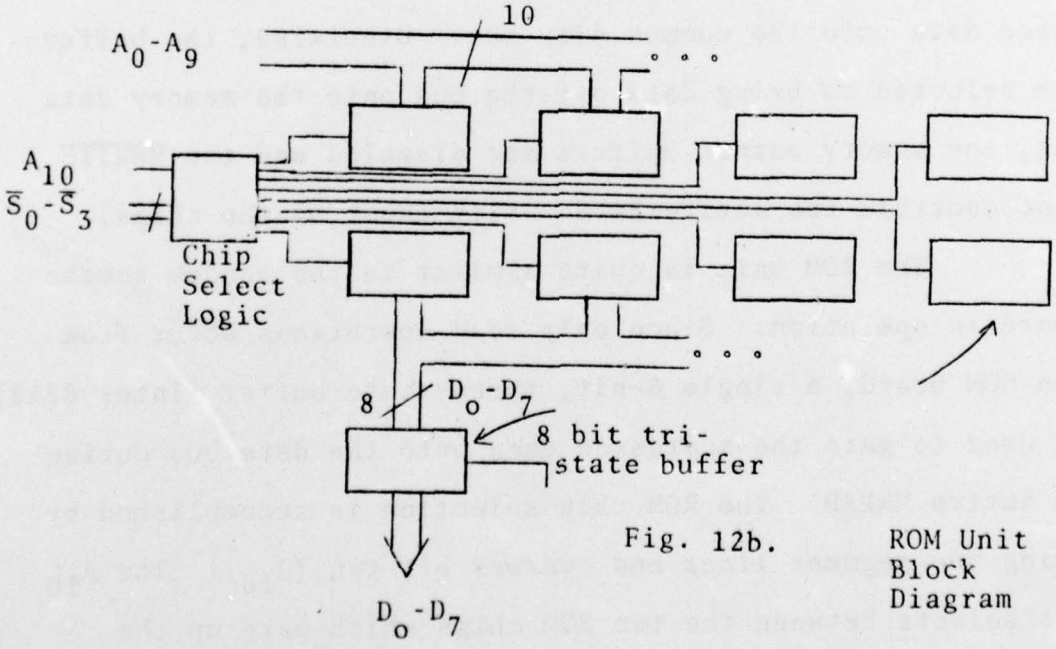


Fig. 12b. ROM Unit Block Diagram

An additional 256 bytes of RAM are on the CPU board and provide temporary data storage area (scratch-pad) during operation.

MEMORY READY LINE CONTROL

The access time, or the time an address must be present at a memory chip before the data becomes valid, for the RAM chips is 850 nsec, and for the ROM 450 nsec. Thus, one wait state is needed to access the RAM, while no wait states are required if ROM is used. The Memory Ready Control Logic determines if memory is being accessed, and if so, whether or not a wait state should be generated by bringing the READY line FALSE during the second clock cycle of present machine cycle. Two switches, S1 and S2 on the CPU board, allow the operator to select between use of only scratch pad memory (usually used only during CPU checkout), a random access main memory and a read only main memory. Inputs from these switches determine the READY line control generated.

DATA PROCESSOR CONTROL SUBASSEMBLIES

The user interface is made up of three printed circuit cards, two subassemblies for computer control and one dedicated to an operator interface.

A control dialog is established with the central processor utilizing one of two possible techniques. The

first method is a simple toggle of an existing control line tied directly to the CPU. These lines, READY, HOLD, INTE, etc., are polled status lines wire "ored" to the 8080A. This method is primarily employed within the two computer control subassemblies. The second technique is to present eight bits of flag data to an interface device (8212) or (8216). This device holds the flag data until serviced by a polling subroutine in software. This interface has been found to be optimum in the circumstance where a dialog is necessary with the software. In the case of the operator interface, large amounts of process information are provided by the operator, to the computer, through switch settings tied directly to several of these interface ports.

Throughout the design of this interface, several basic functions have been utilized repeatedly. The "Hall" effect push button switches are a standard open collector output. Because of the 1 μsec rise time, the output of the push button device is pulled up with a 1K ohm resistor at the input to a Schmitt trigger device (7414) to improve the rise time. A standard configuration, D-type, rocker arm latch is employed to hold the desired switch status. As the input to the latch is grounded through the open collector, the latch will toggle and assume the opposite state each time the button is depressed.

This particular switch interface facilitates software interrupt or reset under program command.

Control Decode

The Control Decode Assembly contains the essential electronics for hardware control of the 8080A central processor, and together with the Data Interface (A-9), form the basic computer interface.

Physical design constraints force the utilization of a synchronous interface with the Intel 8080A. That is to say that all control must be synchronized with both clock waveforms ($\emptyset_1$, $\emptyset_2$) and the SYNC pulse output by the CPU once each machine cycle. For example, to place the machine in a WAIT state, it is necessary to recognize the existence of both $\emptyset_1$ and SYNC at the first of machine state (T2) of a given machine cycle. The READY line must then be taken low before the trailing edge of $\emptyset_2$ clock. In all of the descriptions that follow, reference should be made to the appropriate schematic diagram.

As described above, the common switch interface configuration is a combination of the open collector switch output pulled up in front of a 7414 and driven into the clock input of a "D" flip flop.

ZA1, B1, C1 of A-10 form a status register, the output of which determines the operational mode of

the central processor. With the exception of the three-state, or Hold mode, control of the "Ready" line is utilized in program STEP, stop-on-address (SOA), WAIT and RUN. A "RUN" mode is defined by forcing the "READY" line to a high state.

Careful synchronized recognition of the SYNC and clock waveforms by ZD1 facilitates the single step and breakpoint functions. ZP1, R1 and A4 are clock pulse generators provided to control the READY line in the desired mode.

In addition to these essential control elements, there also exists a set of lamp and line drives for indication of the controller's status.

Basically, the operation of the controller is configurated around the existence of the SYNC and $\emptyset_1$ waveforms. The occurrence of these two signals defines the beginning of a machine cycle. From this point, a number of operational decisions may be made. If the machine is in the on SOA mode, and the desired address is on the address bus, the (A=B) line will toggle high. The existence of (A=B) indicates that the desired 16-bit address, as selected by the operator, has been found. A=B, the proper mode selection, SYNC and $\emptyset_1$ will force the READY line low. The machine will halt and display the operand or data stored in the selected address. If

it is desired to place the machine in a WAIT state, depressing the WAIT control releases the disable on gate ZO1 and facilitates a CPU halt at the next occurrence of SYNC and $\emptyset_1$. In a single step mode (i.e., WAIT lamp lit only) a STEP command resets the READY line high and clears the STEP input latch, ZP1. The machine will execute the remaining portion machine cycle and halt again. This facilitates stepping through the execution of the program to assure proper operation.

There is no preventive maintenance required on this subassembly.

Data Interface

The primary function of the Data Interface is to provide address and data bus register files along with the comparator bus for the Stop-On-Address (SOA) function.

Each 4-bit segment of the address is interfaced to a 74193 counter to provide increment and decrement capability. The physical switch interface is made as described earlier (i.e., open collector to 7414 to 7474). Each time an address button is depressed, the new data are loaded into a 4-bit counter. The output of the counter is fed to a three-state buffer (8216), to a bus selector 74157 and to a 7485 comparator which compares the counter data with bus data through the 8216.

Each 4-bit segment of the address has precisely the same interface (i.e., counter, buffer, comparator and selector).

Based on the status of the control lines, AS, AD, DS, and DD, the counter/register is either outputting data to the bus or bus data are being input for display and comparison. The output from the comparison bus is the desired (A=B) logic level utilized in SOA.

The only difference in the data portion of the system is that the counter and 7485's have been removed. Input data are held in the switch register and the sense of control lines DD and DS determine whether bus or switch data are presented to the operator on the data lamps.

Again, as indicated on the schematic diagram, a set of lamp drivers is also provided for data display.

Operator's Interface

The desired system operational configuration is established through the Operator's Interface.

This subassembly, with the exception of the switch interface, is totally under software control. The switch interface, as shown in the schematic, is the same as has been described earlier. The outputs from the various latches are driven into lamp buffers and to an 8212. The 8212 is the basic input/output device in an

Intel 8080 system. The desired system configuration, as established by the operator, is presented to the input of an 8212. The 8212 and 8216 interface devices may be considered to be peripherals that exist on the parallel data bus. And as with any parallel (pipeline) machine, there may be a large, but finite, number of these devices tied to the bus structure. In general purpose machines, these devices may take the form of printers/plotters or other user oriented output devices. Each of these devices is polled in turn, and the data found therein placed in memory. In this particular circumstance, a large amount of operator selected switch data is held for retrieval.

In addition, the CPU may also write data to an interface device. This particular configuration is utilized for the TIL311 visual display, wherein internal program status and test results are written into the two digit display for operator recognition.

Virtually all of the Operator's Interface is comprised of this type of interface. Operational data, desired to be entered into memory, is presented to the input of an 8212 where it is read when the program falls through the polling routine.

POWER SUPPLIES

The processing system requires six power supply voltages, ±15, + 12, ±5, -5 (1amp). The ±15V source supplying

the analog components and the +5 source supplying the TTL components coexist in a single fused power supply manufactured by Trio Laboratories. This power supply is rated at 1A for the ±15V source and 12A for the +5V source. Furthermore, the +5 source has a remote sensing capability on its voltage regulator allowing a maximum of 5% voltage drop in its output leads. The 12V source is supplied by a modular high efficient power supply, rated at 800mA, manufactured by Semiconductor Circuits, Inc. Similarly, the -5V power supply is another high efficiency supply rated at 800mA, also manufactured by Semiconductor Circuits. The +5V (lamp) power supply consists of a 5V transformer rated at 10amp in conjunction with a 12amp full wave bridge rectifier. This supply is regulated by a 6.2V zener diode and a 12,000 μf capacitor. The +5V (lamp) is used only to drive the indicator lamps located in the front panel.

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The Remote Sensing Center at Texas A & M University is conducting studies for the Naval Surface Weapons Center to develop a real-time, special purpose radar data processor. The purpose of this processing system is to provide ice type identification using radar scatterometer measurements. This document provides information for the operation and maintenance of the developed processor system.

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The REMOTE SENSING CENTER was established by authority of the Board of Directors of the Texas A&M University System on February 27, 1968. The CENTER is a consortium of four colleges of the University; Agriculture, Engineering, Geosciences, and Science. This unique organization concentrates on the development and utilization of remote sensing techniques and technology for a broad range of applications to the betterment of mankind.